R42

Third generation Large Area Professional DSC CCD process and design technology

C.Draijer (cees.draijer@dalsa.com), W.Klaassens, H.L. Peek, H.Stoldt, B.G.M.Dillen, J.T.Bosiers.
DALSA Professional Imaging (DPI), High Tech Campus 12a M/S01 5656 AE, Eindhoven, The Netherlands
Tel: +31 40 2743957, Fax: +31 40 2744090

Introduction

The ongoing demand for even more pixels in large-area CCD imagers for professional DSC applications requires downsizing of the pixel on the one hand and, at least, maintaining the performance of the previous pixel generation on the other hand. Moreover higher-speed read out is required to maintain the frame rate. We will show that with improved process technology (see Table 1) and new layout options, this challenge can be met. In this paper a 7.2 x 7.2 μm^2 pixel is presented, which is manufactured in a new large-area process technology. Although it is obvious that smaller pixels will have a smaller charge handling capacity, the signal to noise ratio (SNR) should be maintained over a wide range of operating modes to assure an excellent ISO performance of the DSC camera (see figure 1). With process features like membrane poly-silicon gates together with Tungsten strapping in combination with an advanced lithographic stitching process and an improved amplifier, a high-performance large-area sensor has been realised as a research vehicle with this new pixel (see figures 2, 3, 4). To accelerate the pixel readout, the RC-times of the interconnections have been reduced and (multiple) high-bandwidth, low noise amplifiers have been applied.
In general smaller pixels, especially over very large areas, pose serious challenges to maintain the production yield since the distances between critical structures are reduced. By a novel design concept this challenge for large area CCD's with small pixels could also be met. The improved technology also gave the opportunity to add extra on-chip design features like clock pick-up structures for a high-speed horizontal register, and binning.

Process Technology options

Membrane poly-silicon technology [1] with dual-metal layer and shunt wiring was demonstrated in small-pixel devices for consumer applications. These imagers have an image diagonal typically 2/3 inch [2] and smaller. However the application of this technology to large area CCD's challenges the standard process modules of the current large-area CCD process technology.
First of all the technology should support the 'stitching' of process layers [3] . Although this has been successfully applied in other dedicated large-area CCD process technologies, this concept had to be transferred to the membrane poly-silicon technology. The stitching of layers during resist illumination requires under- and over-illumination compensation structures to prevent deviations in (resist) line widths. All these compensation structures were reconsidered and optimised for the new Large-Area CCD technology.
Secondly, for yield improvement, the poly-silicon layers receive an extra etch step to eliminate possible residues caused by particles, to reduce the risk of shorts (see figure 5).
And finally, large-area devices require an excellent uniformity over the wafer to prevent shading effects. The design rules and process conditions have been critically reviewed and optimised to maintain the excellent uniformity also in this new large area technology.

---

[1]: H.Peek et al, " An FT-CCD imager with true 2.4x2.4 μm^2 pixels in double membrane poly-Si technology". IEDM Tech. Dig.1996, pp. 907-910
[2]: Bosiers et al," A 2/3" 2-M pixel progressive scan FT-CCD for digital still camera applications", IEDM Tech. Dig. 1998 pp.37-40
[3]: Kreider et al," An mK x nK modular image sensor design. ", IEDM Tech. Dig pp. 155-158

Design options

The new technology allows both new design measures to optimise the yield, and extra opportunities to extend the functionality. For yield optimisation, the vertical straps connecting the clocks have been bundled to reduce the number of possible critical shorts by more than a factor of 4 (see figure 6). The new technology option enables the insertion of clock pickup circuits in the horizontal register. These circuits make high-speed applications (>25MHz) possible, by reducing the RC-times of the register (see figure 7). The performance of the amplifier also benefits from the new technology. Reducing the parasitic capacitance increases the amplifier conversion factor. From this reduction also the noise performance will benefit, without compromising on bandwidth. Finally, given the extra metal and thick poly straps (see also figure 4), a concept of on-chip binning for high-speed preview is within reach.

Results

The main features of the three generations of large area technologies are given in table 2. The most striking is the fact that the third generation technology gives higher sensitivity in green. Also the positive effect of lower parasitic capacitances due to the smaller contact hole size is visible in the noise and conversion factor performance. The Dynamic Range is reduced slightly over the pixel generations, but the much lower noise of the amplifier keeps in pace with the maximum charge reduction. The charge storage capacity, expressed in electrons per square micron (figure 8), remains high while the pixel area decreases significantly. The Vertical Anti Blooming ensures excellent high light handling. Although the processes themselves are not very different considering the dark current generation, a further reduction of dark current is realised due to incremental process improvements.

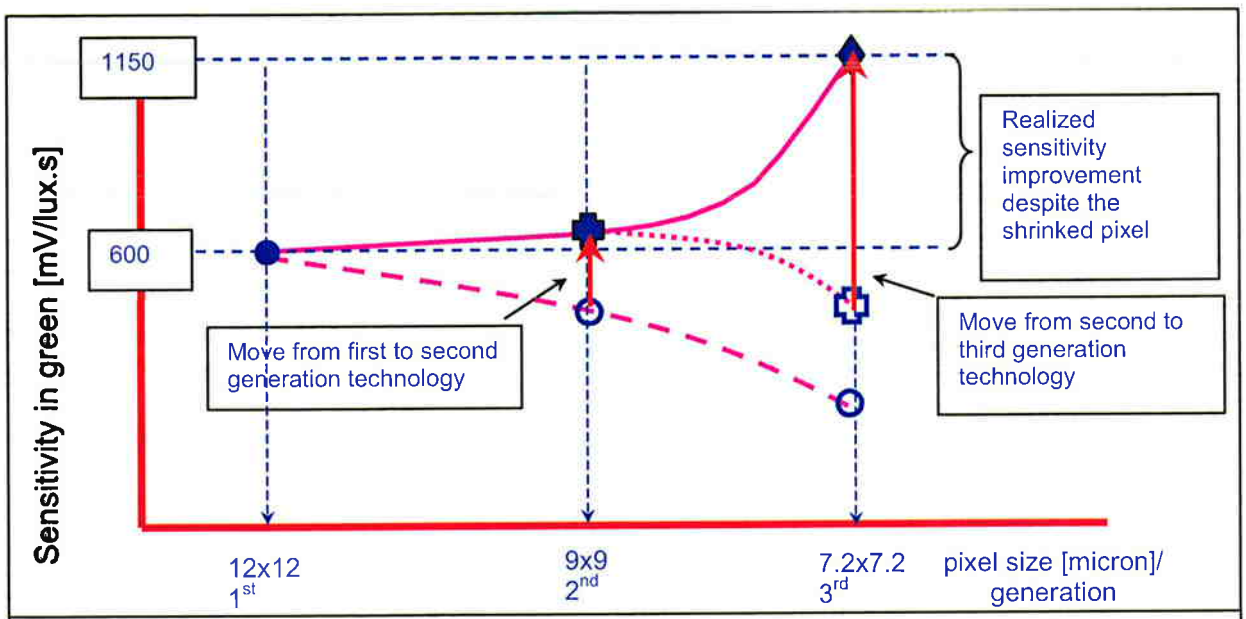

Figure 1: The relation between process generation and the sensitivity in green. The circles give the realized sensitivity for the first pixel generation and the anticipated performance for successive pixel generations (open circles) in the 1st generation technology. The crosses denote the sensitivity while using the 2nd generation technology. The diamond denotes the realized performance by using the 3rd generation technology.

Figure 2: A scene taken with the research vehicle with a 7.2 x 7.2 μm^2 pixel, processed in the 3rd generation technology.

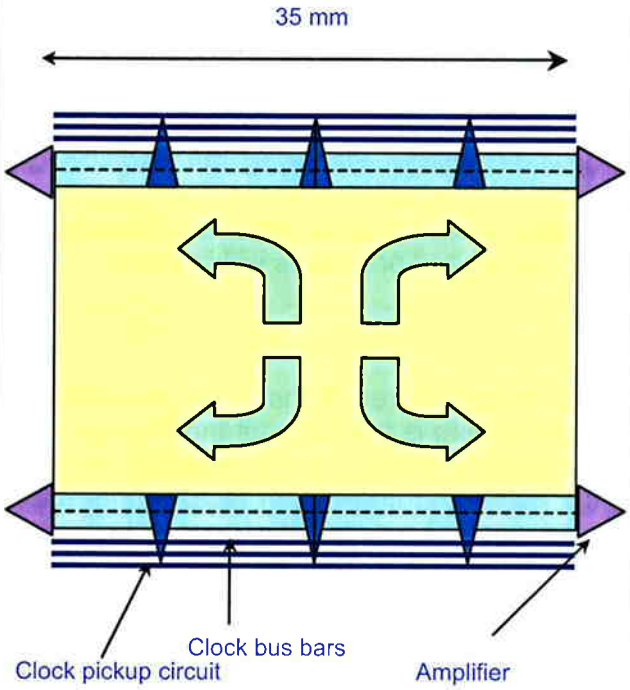

Figure 3: Schematic view of the research vehicle, which can be read out over 4 amplifiers, one at every corner. The pickup circuits reduce the RC times over the 35 mm long register.

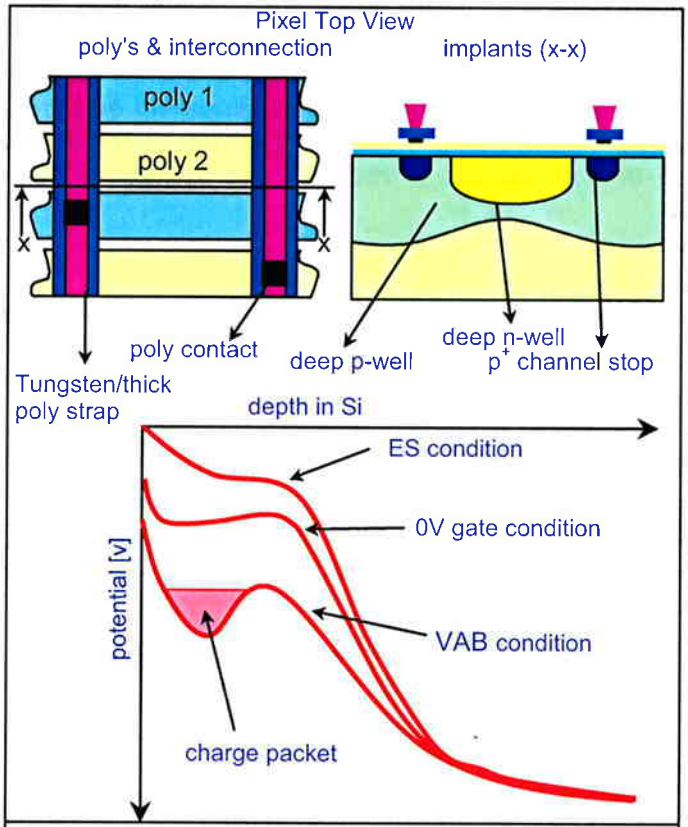

Figure 4: The 7.2 x 7.2 μm^2 pixel architecture, Featuring thin poly gates, Thick poly straps with Tungsten (W) interconnect. The pixel has Vertical Anti-Blooming (VAB) and accommodates Electronic Shuttering (ES). The charge capacity is 60 ke^-

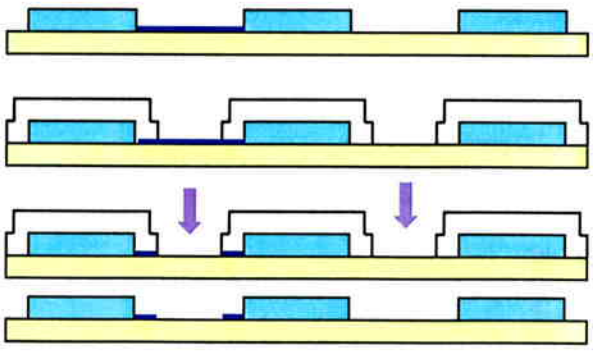

Figure 5: The extra etch step for yield. A short between two poly gates is a potential yield loss. After the application of a protective resist on the gates, a second etch step eliminates the short.

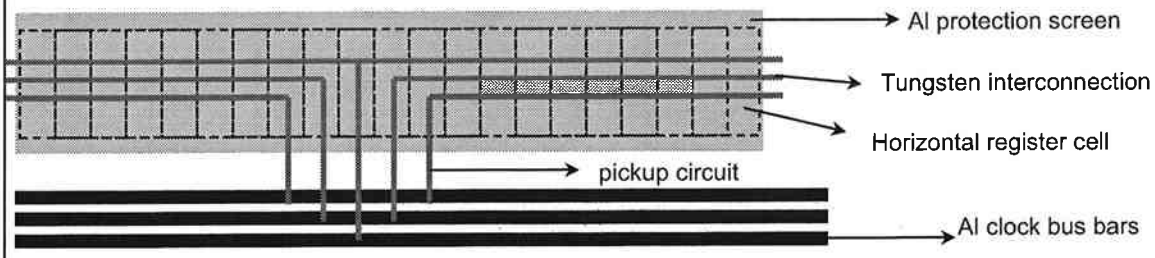

Figure 7: Conceptual design of the 3-fase C-clock pickup circuit to enable a high speed register up to 40 MHz. The pickup circuits supply the clock signal at the bus bars to the tungsten interconnect above the register cells. The register is screened from light by an Al protection screen.

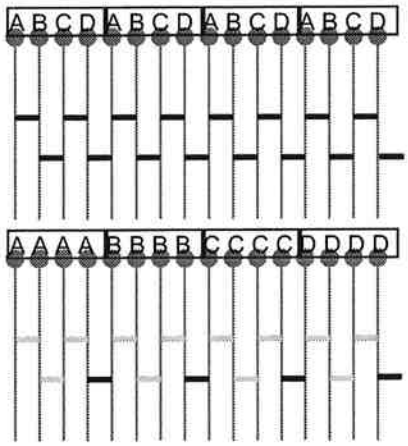

Figure 6: Reduction of critical shorts (━) by a factor of 4, due to bundling the 4-phase clock straps

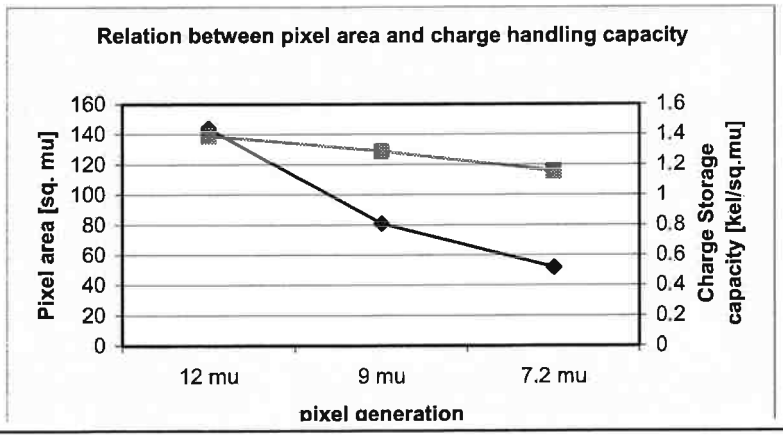

Figure 8: The relation between charge storage capacity and pixel area.

Table 1: Large Area Technology features	1st generation	2nd generation	3rd generation
poly silicon gate electrodes	3 poly, standard	3 poly, standard	2 poly, membrane
Metal layers	1	2	2
Contact hole size [µm^2]	2 x 2	1 x 1	0.6 x 0.6

Table 2: Typical Technology performance	1st generation	2nd generation	3rd generation
Typical DSC pixel size [µm square]	12x12	9x9	7.2x7.2
Green sensitivity[1] [mV/lux.s]	600	650	1150
ACF [µV/e$^-$]	8	20	40
Noise[2] [e$^-$]	38	30	18
Qmax [kel]	200	105	60
Dynamic Range	74 dB	71 dB	70 dB
Charge storage capacity [ke$^-$/µm^2]	1.39	1.29	1.16
Dark Current @ 60°C [nA/cm^2]	0.3	0.2	0.1
Horizontal clock cap [pF]	200	200	200
Bandwidth[3] [MHz]	140	110	130
Fill Factor[4] [%]	82.5	77	72

notes:
[1] Sensitivity measured with IR filter
[2] Noise in full bandwidth @ 25 MHz after CDS
[3] Measured at –3dB
[4] Geometric Fill-factor, taking into account the presence of a colour separation grid